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FRONT-END DATA PROCESSING USING THE BIT-SLICED MICROPROCESSOR*

by

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ABSTRACT

A state-of-the-art computing device, based upon the high-speed bit-sliced microprocessor, has been developed into hardware for front-end data processing in both control and experiment applications at the Los Alamos Scientific Laboratory. The CAMAC Instrumentation Standard provides the framework for the high-speed hardware, allowing data acquisition and processing to take place at the data source in a CAMAC crate.

INTRODUCTION

A consistent approach to the problems of data throughput, limits on computational capability and unresponsive system software seems to point towards distributed processing. We find these problems plaguing both control and experiment data systems to varying degrees; the control system suffers from computation limits and unresponsiveness, while the experiment data system is unable to process over a few events per unit time owing to rate-bound I/O channels and a compute-bound Central Processor (CPU).

Further, we find that the computer and semiconductor industries have made available processing elements that allow the practical engineering of distributed computing systems (mini- and microcomputers, microprocessors and microprogramming chip-sets). Previous problems of physical size, cost and limited basic capabilities have been either overcome or greatly reduced; we can now select inexpensive, physically compact and highly capable computing devices for use in control or data acquisition systems.

More specifically, we must find an appropriate framework in which to house these processing elements in a distributed sense. The framework must allow free communications between a CPU and the distributed processing facilities, while allowing the distributed processors freedom to interact in the control or data acquisition application.

A set of system elements, together with a usable framework for distributed processing, is described. The system elements are being used in both distributed control and data acquisition applications at the Los Alamos Scientific Laboratory (

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A FRAMEWORK FOR DISTRIBUTED PROCESSING

Many large national and international laboratories have traditionally utilized the CAMAC instrumentation standard[1] in equipment or facility control and experiment data acquisition systems. The CAMAC standard now allows multiple (or Auxiliary) Controllers[2] to be placed in each CAMAC crate. This feature, in addition to the previous capability of placing multiple crates on a CAMAC Highway, is an example of a distributed processing framework that is being used at LASL.

A demanding test-bed for such a framework exists in the Accelerator Technology Division, for accelerator control systems, and at the Clinton P. Anderson Meson Physics Facility (LAMPF), for both beam-line control and high-rate experiment data systems.[3,4] In the former case, the CAMAC Serial Highway connects crates containing Auxiliary Controllers and medium-speed processing elements, while in the latter case the CAMAC Parallel Highway contains crates with Auxiliary Controllers and high-speed processing elements. However, both applications are based upon the concept of a multi-microprocessor CAMAC Auxiliary Controller[5] developed by the author for the Daresbury Laboratory, England, for use in high-rate experiment data acquisition.

Finally, the communication link to a CPU, from intelligent multiple controllers in a CAMAC system, can be either over a standard CAMAC Highway or over industry-standard data communications links. In either case, the advantage of making the distributed processing framework in CAMAC can be tied directly to the vast numbers of device interface modules available in CAMAC and to the close coupling between modules and distributed processing elements possible in a CAMAC crate.

FRONT-END PROCESSING

Experiment planners faced with high data rates and complicated event injection criteria

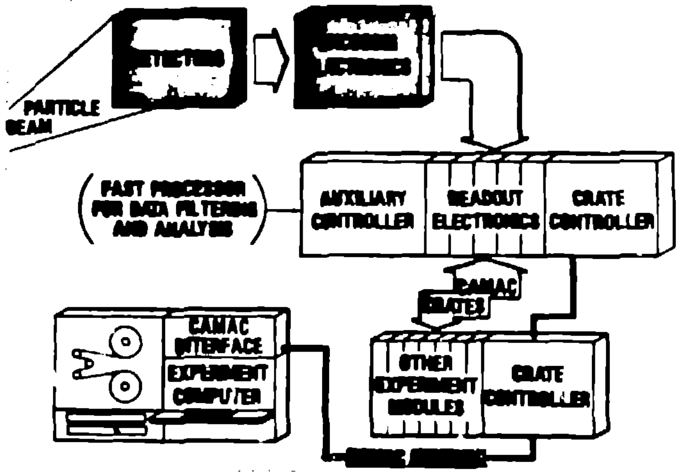

Fig. 1.
Front-End Processing in a CAMAC System.

will be especially interested in the techniques of front-end and distributed processing discussed in this paper. Such an experiment data system is illustrated in Fig. 1 and shows a detector and encoding electronics (usually done in Schottky TTL or ECL integrated circuit technology and, therefore, very fast), a front-end processing device consisting of a CAMAC Auxiliary Controller in a standard CAMAC Highway system and a central experiment computer.

The constituent elements of an Auxiliary Controller are extremely important; secondary trigger generation, computed data-cuts, data filtering or more detailed data analysis is determined directly by the capability of the Auxiliary Controller. A designer can effect the processing capability of an Auxiliary Controller through the type of computing elements included in the Controller and the way in which the computing elements are able to interact with CAMAC modules. Of course, an Auxiliary Controller designed for use in front-end data processing applications must have, as a primary member of the controller hierarchy, the fastest processor element available; today, this can only be achieved by using the techniques of microprogramming and the bit-sliced, bipolar microprocessor chip-sets currently available from only a few semiconductor manufacturers.

Through the use of bit-sliced microprocessor technology, we are able to realise computation rates from 15 to 20 times that of the nearest microcomputer or single-chip microprocessor. Such an increase in the execution speed of processing elements at the front-end, or data collection end, of an experiment makes possible extremely complex secondary triggers, data cuts, filtering and analysis in a stored program sense. This is always much easier than a hardware implementation, albeit somewhat slower; a hardware approach to front-end processing is limited by what is practical to implement in the sense of realisable logic, however.

AN AUXILIARY CONTROLLER FOR FRONT-END PROCESSING

A CAMAC Auxiliary Controller[5] that has been optimised for high-speed front-end processing applications is shown in Fig. 2 and in block diagram form in Fig. 3.

The prototype Auxiliary Controller elements are shown in Fig. 2. Each element is contained on a CAMAC module and its mechanics, and in most cases only takes power from the Dataway. The Controller elements are constructed on CAMAC modules, in part to reduce the number of cables, connectors and power supplies required, while creating the closest possible coupling between the Auxiliary Controller and the instrumentation modules. The controller Q-Bus is located on the front of each module and is connected together by a front mounting "mother-board" when installed.

The block diagram depicts the several busses in the system—the CAMAC Dataway, the Auxiliary Controller Bus (ACB) and the internal or LSI-11* Q-Bus—and each element of the Auxiliary Controller (as a block) connected to the Q-Bus. As mentioned, the controller is based upon the LSI-11/2 microcomputer and the associated interface bus, or Q-Bus. Other controller elements are interfaced to this asynchronous handshake data transfer bus, and in some cases to the Dataway.

The various memory elements available are MOS dynamic RAM (16K), 200-ns RAM, 50-ns RAM and

*Trademark - Digital Equipment Corporation.

Fig. 2.
Prototype Auxiliary Controller Modules.

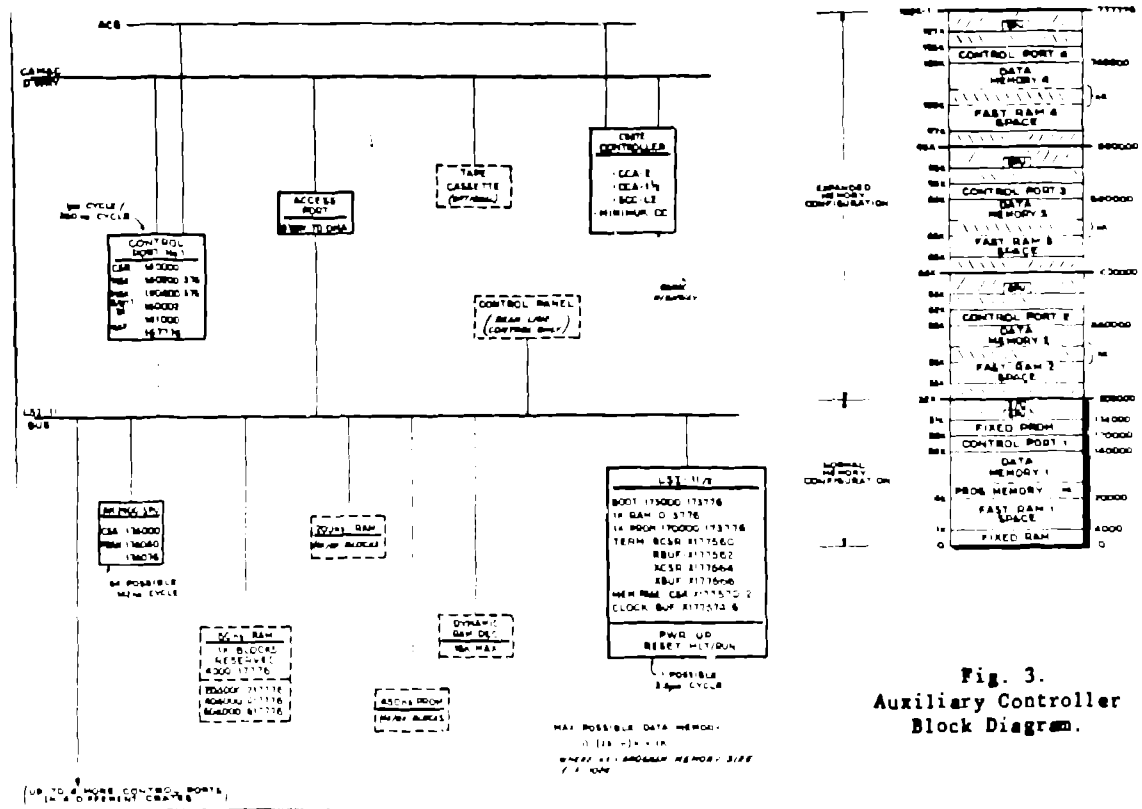

Fig. 3.
Auxiliary Controller
Block Diagram.

erasable PROM. When the new LSI-11/23† becomes available, single boards containing a 64K MOS dynamic RAM will be usable without modifying the Controller.

Two Controller elements serve to connect the unit to the CAMAC Dataway. The Dataway Access Port allows a central computer to communicate with the Controller Q-Bus from the Dataway (Auxiliary Controller memory loading or readout); the Control Port provides the Auxiliary Controller with the means to initiate Dataway cycles. Additionally, the Control Port arbitrates for mastership of the Dataway over the Auxiliary Controller Bus,[2] and it may be used to extend the Auxiliary Controller to four other crates. The port is able to short-cycle the Dataway (300-ns cycle, without strobe S2) and can execute multiple cycles, as described in Ref. 2. The latter features are especially useful in front-end processing applications.

THE HIGH-SPEED PROCESSING ELEMENT

The device that enables the Auxiliary Controller to become an effective front-end processing device is the AM-2900, Special Processor Unit (SPU). This element uses the AMD-2900 family[6] bipolar, bit-sliced microprocessor chip-set in a familiar Wilkes[7] microprogramming structure. The SPU block diagram, shown in Fig. 4, indicates how the microcode sequencer (AM-2910) generates the control memory address, based upon feedback from the current instruction held in a microinstruction pipeline register.

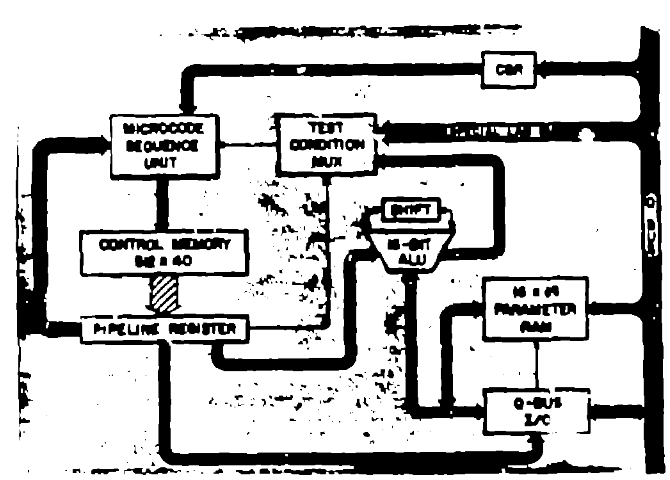

Fig. 4.
Special Processor Organization.

†A new product announcement by DEC (January 1979).

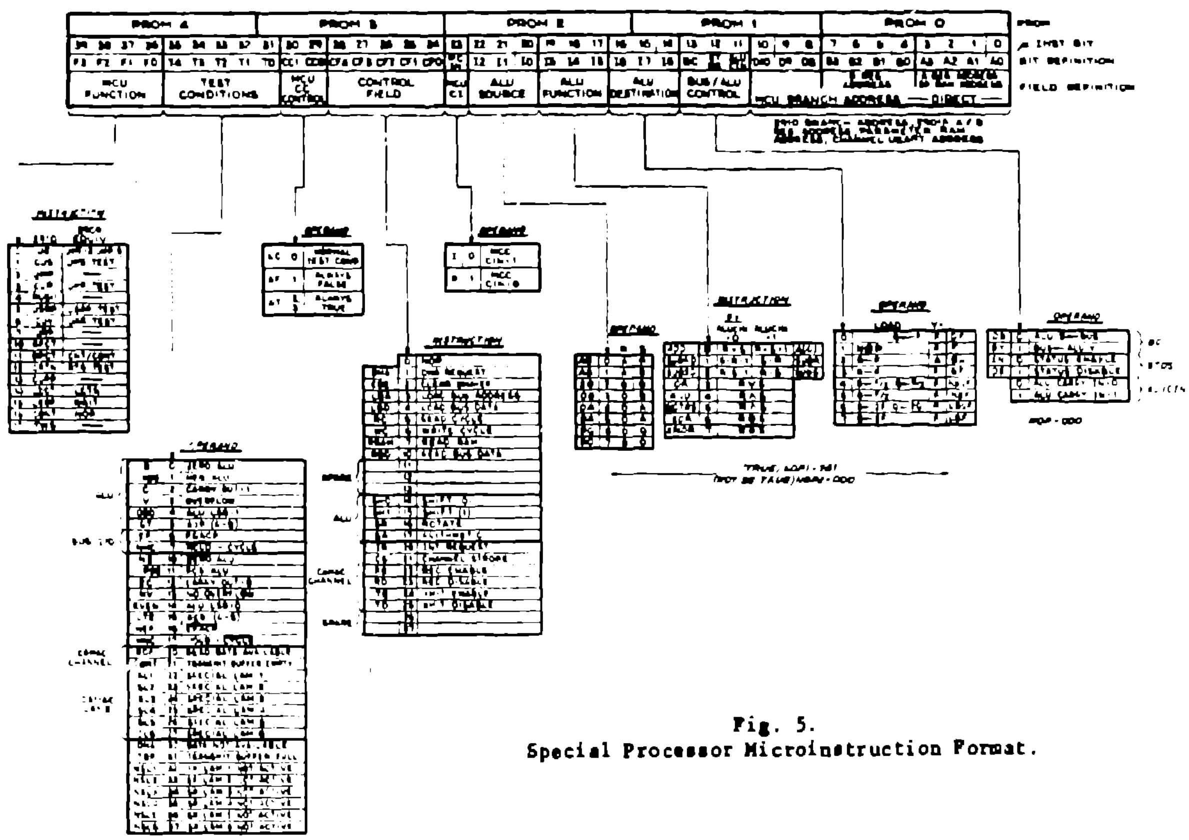

Fig. 5.
Special Processor Microinstruction Format.

A Schottky TTL Arithmetic Logic Unit (ALU) is a 16-bit-wide unit made up of four, 4-bit ALU slices (AM-2901B). The facility is capable of executing microinstructions from a 35-ns fuse-link PROM control memory at a 7-MHz clock rate (142-ns cycle time). The SPU is made useful to the Auxiliary Controller through the interfaces shown on the right side of the Fig. 4: The CSR (Control-Status Register) provides SPU status to the LSI-11/2 and a means to start the SPU at a specific control memory address; a set of six special LOOK-AT-ME (LAM) signals is mapped from the Dataway, through the Control Port, to the SPU for testing and subsequent use in address control; a 16-bit by 16-register parameter RAM serves as a "mail-box" between the LSI-11/2 and the SPU—the RAM allows the SPU to be used as a firmware subroutine facility with passed parameters going into the RAM on execution; finally, a Q-Bus interface allows the SPU to request mastership of the Q-Bus and initiate both Read (Data-In) and Write (Data-Out) cycles—the Q-Bus cycle times accommodate to the controlling devices and reflect the much faster cycle time of the SPU over the LSI-11/2.

The microinstruction format, shown in Fig. 5, includes both the AMD-2910 microcode sequencer instructions and the AMD-2901B ALU instructions, in addition to several fields devoted to other facility options. The reader should note that the microinstruction structure is a combination of both vertical and horizontal implementations; many operations are mutually exclusive and, therefore, dictate a shared microinstruction field.

Microcode development for the SPU is aided by a cross Meta-Assembler from MicroTec Corporation.* Following a field and mnemonic definition phase, SPU code is written much like any conventional assembler, except that a line of code may contain a concatenation of up to three operation fields. A minicomputer development station, aided by a disk operating system, allows the easy transfer of formatted object files to an SPU control memory simulator for microcode debugging prior to programming the fuse-link PROMS. During debug, the SPU operates on a 1-MHz clock rather than the normal 7-MHz clock. Development of LSI-11/2 code for the rest of the Auxiliary Controller is done on the development station using the common utility programs available on the disk operating system. Object code transfer takes place over the CAMAC Dataway to the Dataway Access Port.

APPLICATIONS AND CONCLUSIONS

The CAMAC Auxiliary Controller described is the distributed processing element in both a beam-line control application[4] and a high-rate experiment in the LAMPF experimental area. The unique Special Processor Unit has made the

*MicroTec, Sunnyvale, California 94088, USA

Controller a very necessary part of Experiment 394, "Applications of Proton Computed Tomography" due to run on LAMPF P3 beam line in late May 1979. The Controller will perform the following operations: During the 500-μs LAMPF beam pulse, the SPU will readout up to 250, 16-bit events from a Multiwire Proportional Chamber (MWPC)/range-telescope encoder.[8] The Auxiliary Controller remains under the control of the SPU following the beam pulse and histograms the MWPC data, calculates the mean of these data, histograms 11 range-telescope arrays (based upon MWPC data-bins on either side of the calculated mean) and calculates the mean of each array. A data compression of 10:1 is achieved by doing the analysis between beam pulses of the LAMPF beam. The compressed data is finally reduced on a larger computer to reconstruct the cross-sectional view of an object scanned by the proton beam.

We have seen how distributed processing can be implemented in a framework based upon the CAMAC instrumentation standard, together with the elements of a CAMAC Auxiliary Controller. Specifically, a high-speed processor coupled to the Auxiliary Controller provides the means by which front-end processing can be implemented in a realistic way. The specific application to Computed Proton Tomographs is typical of the possible uses of such techniques and devices based upon state-of-the-art electronics.

ACKNOWLEDGMENTS

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